Design and Analysis of the on-chip Power Delivery Network for Energy Efficient Designs

Kyle Craig
Department of Electrical and Computer Engineering
University of Virginia

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Abstract

In digital integrated circuit design energy efficiency has become one, if not the, most important metric. From low performance sensor nodes to high performance CPU's and servers, energy efficiency is driving design. Two conventional techniques for improving energy efficiency are dynamic voltage and frequency scaling (DVFS) and power gating. Both these techniques modify the power delivery network to improve energy efficiency. DVFS uses off-chip DC-DC converters to scale voltage, leveraging the quadratic relationship between energy and voltage. Power gating inserts a transistor in the power delivery network, effectively removing a component from the power delivery network to reduce overall leakage. An emerging technique to improve energy efficiency is subthreshold operation. This is an attractive option due to the drastic reduction in supply voltage. However, this comes at the cost of an exponential decrease in performance. Subthreshold operation is best suited for low performance applications. This work focuses on design and analysis of new energy efficient on-chip power delivery network optimizations that do not rely on costly off-chip DC-DC converters while still leveraging quadratic energy savings and enabling subthreshold operation.

In this work, we first explore two power delivery network optimizations that do not rely on off-chip DC-DC converters. Instead, they modify the on-chip power delivery network much like power gating, but still provide dynamic voltage scaling. Next, we explore architectural and power delivery network optimizations that are required to enable subthreshold operation. Next, we will use commercial power delivery analysis tools to evaluate the impact our proposed on-chip power delivery network optimizations have on the entire power delivery network. Finally, we develop a scripted infrastructure to enable rapid design of energy efficient designs.

1. Introduction

1.1 Motivation for energy efficient operation

In modern digital integrated circuit design one of the largest focuses of research is in energy efficient CMOS design. Energy efficiency is defined as completing an application's workload at the lowest energy. A wide range of applications exist that are constrained by energy but still require burst of performance, and need to be as energy efficient as possible. The applications can be broken up into two broad categories based on performance, high end and low end. Examples of high end applications are: servers, desktop computers, personal computers, etc. Example of low end applications are: portable media players, smart phones, bio-medical devices, etc.

Both of these categories of applications have their own energy constraints. For example, high end applications are limited by heat dissipation. As the size of the transistor continues to scale allowing for more transistors to fit on-chip, the heat density has become prohibitively large. Historically, this led to an increase in the cost of cooling and the shift away from increasing single core processor frequency to slower multicore processors on the same chip in order to improve performance. However, low end applications are limited by life time concerns associated with battery and battery-less energy capacity. To improve energy efficiency two conventional techniques have become widely adopted in industry, dynamic voltage and frequency scaling and power gating [1][2]. A third emerging technique is to operate with a supply voltage at, or below, the transistor's threshold voltage.

1.2 The on-chip power delivery network

The power delivery network is a large system consisting of many different components. Figure 1–1 below shows a simplified model of the power delivery network. In many commercial systems the voltages generation is done through DC-DC converters on the printed circuit board (PCB). There are resistances, inductances, and capacitances (RLC) associated with the PCB, the package and the chip itself. For the purpose of this work, we will focus on modifications to the on-chip power delivery network to enable energy efficient design. To evaluate the impact of our energy efficient design on the entire power delivery network, we will use a simplified model similar to Figure 1–1.

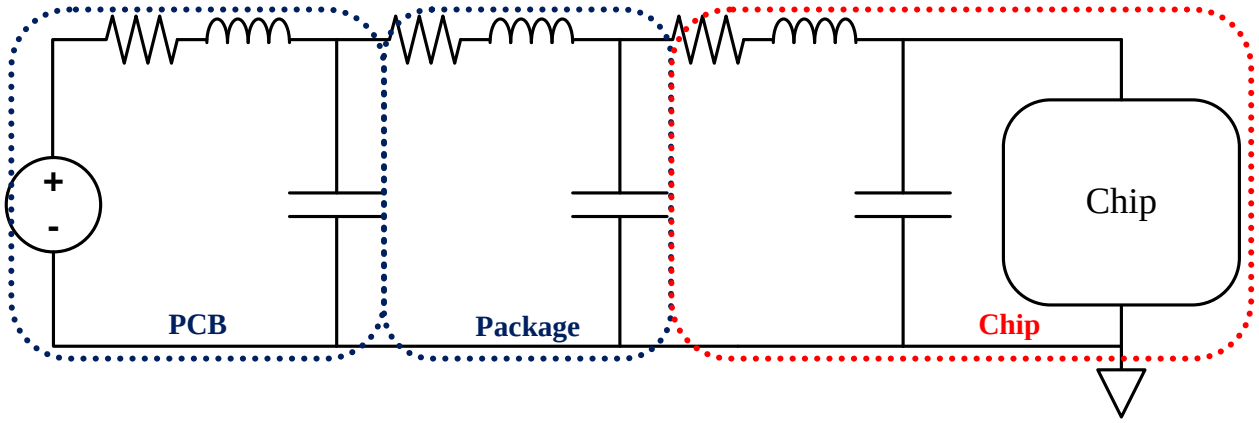

Figure 1–1. Simplified model of the power delivery network

1.3 Prior art

The strongest knob for improving energy efficiency is to reduce supply voltage, V_{DD}. Energy per operation is defined below in terms of dynamic and leakage energy,

$$E_{op\_dynamic}(V_{DD}) = C_L(V_{DD}) * {V_{DD}}^2 \qquad \text{eqn. 1–1}$$

$$E_{op_{leakage}}(V_{DD}) = V_{DD} * I_L(V_{DD}) * t_{op}(V_{DD}) \qquad \text{eqn. 1–2}$$

where $C_L(V_{DD})$ is the circuit's load capacitance as a function of V_{DD}, $I_L(V_{DD})$ is the leakage current as a function of V_{DD}, and $t_{op}(V_{DD})$ is the delay of the circuit as a function of V_{DD}. Reducing supply voltage can lead to a greater that quadratic savings in energy per operation when considering both dynamic and leakage energy. Dynamic energy is the energy consumed by the charging of internal load capacitances, caused by transistor switching. Leakage energy is the energy that is consumed through transistors that are "off" and not switching. Leakage occurs due to a transistor not being an ideal device, and having a small amount of quiescent current. Two conventional techniques to reduce dynamic and leakage energy are dynamic voltage and frequency scaling and power gating, while and emerging technique is subthreshold operation.

Dynamic Voltage and Frequency Scaling (DVFS)

As previously mentioned, one of the strongest knobs for improving energy efficiency is adjusting the supply voltage, V_{DD}. However performance is proportional to V_{DD}; reducing voltage saves energy at the cost of performance. Dynamic voltage and frequency scaling is a technique that leverages the quadratic energy savings whenever performance requirements allow [1]. As shown in Figure 1–2, a conventional DVFS implementation uses a off chip DC-DC converter to scale V_{DD} when performance requirements change. The method for scaling frequency is outside the scope of this work however a typical method is to use on-chip clock generation, such as phase lock loops (PLLs) control the frequency scaling. DVFS improves energy efficiency by adjusting to the lowest V_{DD}, with the slowest frequency required for a given application. DFVS has been shown to have energy reductions up to 4.5X for various applications [1].

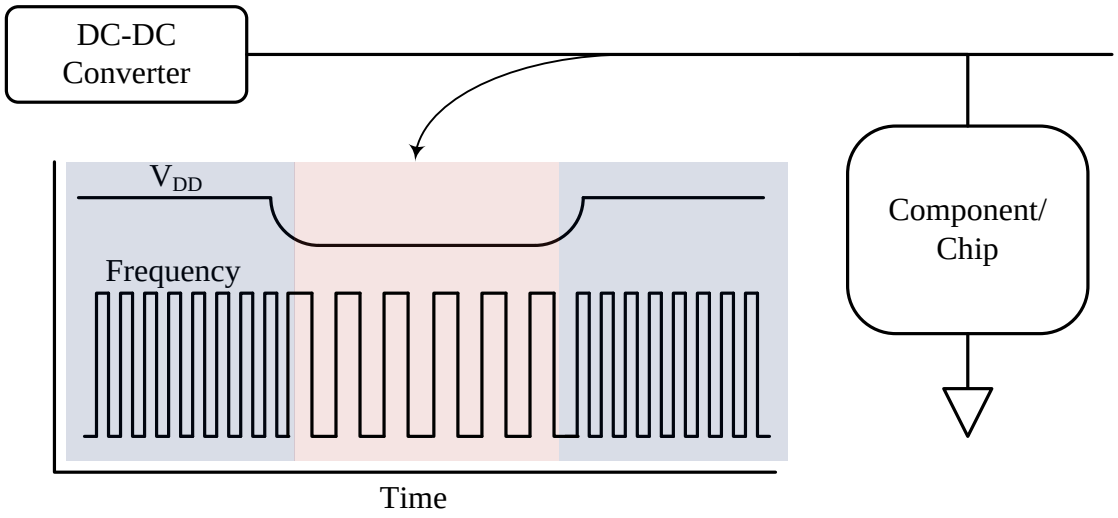

Figure 1–2. Dynamic Voltage and Frequency Scaling

Power gating

Modern commercial processors consist of multiple cores, each being complex with many different components required to execute general purpose applications. For a given application, it is unlikely that all the cores or components will be used. Instead they will be idle and leaking, reducing the overall application energy efficiency. A conventional technique for minimizing leakage, and improve energy efficiency, is to power gate the component or core. Power gating is shown in Figure 1–3. A PMOS transistor is placed in the power delivery network in series between the V_{DD} and component, or a NMOS transistor is placed in series between the ground and core. This creates an intermediate node known as virtual-V_{DD} (or virtual-V_{SS}) as the effective supply to the core. When the power gate is turned off the virtual node will collapse reducing the voltage across the core, reducing the leakage from the component.

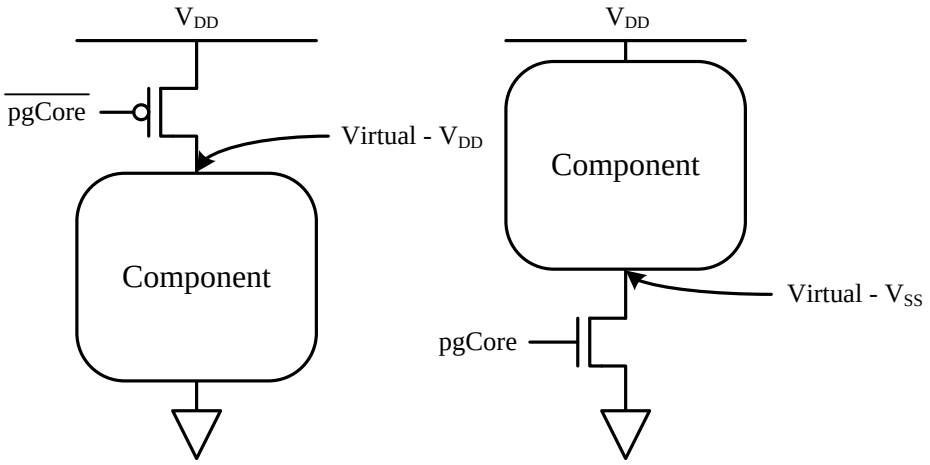

Figure 1–3. (*left*) power gating with PMOS header (*right*) power gating with NMOS footer

Subthreshold operation

A major focus of energy efficient design in academia is to run the entire circuit with a supply voltage below the threshold voltage of the device. This is known as subthreshold operation. The threshold voltage (V_T) is defined as the transistor gate to source voltage differential (V_{GS}) that is required to begin conducting current through the transistor. When V_{GS} is below V_T, the transistor is off, and when V_{GS} is above V_T the transistor is on. Even though the transistor is considered 'off' there is still enough current to charge and discharge internal capacitances and differentiate between the logical 1's and 0's in order to perform digital operations. As stated above energy has a more than quadratic dependency on V_{DD}. However, in the subthreshold mode of operation performance has an exponential, not linear, dependency on V_{DD}. For this reason, subthreshold is best suited for low end performance applications.

1.4 Key design challenges in the on power delivery network

For the purposes of this work four key power delivery network design challenges are going to be considered. These design challenges become apparent when considering the impact of DVFS and power gating on the power delivery network and must be considered when implementing an energy efficient design.

Voltage scaling
There are two key design challenges with the power delivery network are introduced with DVFS. The first one is scaling using DC-DC converters. To scale the chip V_{DD}, DC-DC converters are commonly used. One of the biggest issues with DC-DC converters is the time required to scale voltage for an entire core. This time can often be in the order of tens to a hundred microseconds and limits the opportunity to implement voltage scaling [3].

V_{DD} granularity
The second key design challenge introduced using DVFS is V_{DD} granularity. In multi-core designs, the same DC-DC converter and V_{DD} are often used to power all the cores in the design. This large V_{DD} granularity further limits the opportunity to use DVFS since scaling can only happen when all cores in a design have the same voltage requirements.

IR drop
The next two design challenges with the power delivery network are introduced with power gating. The third key design challenge is IR drop across a power gate. If a power gate is sized too small the transistor will not be able to meet the load current demands of the component. This results in the virtual-V_{DD} value to drop to a lower than desired value, reducing performance and in the worst case a breakdown of functionality. If a power gate is sized too large the leakage energy savings will be reduced.

di/dt noise
The final key design challenge in the power delivery network is di/dt noise. When a power gated component is reconnected to V_{DD} (i.e., power gate turned back on) there is a large rush current that is associated with returning the collapsed virtual-V_{DD} to the nominal voltage value. Since the power delivery network consists of many intrinsic resistances, inductances and capacitances, the rush current creates a ringing noise throughout the power delivery network. Power delivery network noise will reduce chip performance, reducing the maximum frequency.

1.5 Research Goals

The following is the list of research goals of this work,

- Investigate how the on-chip power delivery network can be optimized to improve the energy efficiency of conventional super threshold architectures. Propose new power delivery networks that no longer rely on DC-DC converters to scale voltage.
- Investigate how the conventional super threshold architecture and the power delivery network can be modified to enable subthreshold modes of operation. Propose architecture techniques and power delivery networks optimizations to enable subthreshold operation.
- Analyze how these proposed energy efficient architectures and on-chip power delivery networks impact IR drop and di/dt across the entire power delivery network.
- Propose design techniques to mitigate IR drop and di/dt introduced by the proposed architectures.
- Develop a scripted infrastructure that allows for rapid design space exploration of energy efficient architectures and analysis of the power delivery network.

1.6 Thesis Statement

Energy efficiency is the major focus in modern digital design. However, V_{DD} scaling with off chip DC-DC converters limits the V_{DD} scaling opportunity. New on chip power delivery network optimizations need to be developed to continue improving energy efficiency. The impact of these optimizations also needs to be evaluated in the context of the entire power delivery network.

2. Improved voltage scaling architectures

2.1 Motivation

As previous mentioned, energy efficiency is arguably the most critical metric in modern digital integrated circuit design. Many systems, both high and low end, occasionally require bursts of performance, but their varying workload requirements remain below this upper limit for the majority of their lifetimes. Designing for this worst case performance requirement leads to drastic energy inefficiency in the common case. As mentioned, dynamic voltage and frequency scaling (DVFS) provides the ability to tradeoff performance for improved energy efficiency for varying application. Power gating provides the ability to improve energy efficiency by reducing the leakage energy in idle cores/components. Two of the key design challenges with DVFS are the voltage scaling with DC-DC converters as well as the V_{DD} granularity. We propose two different power delivery network architectures that provide finer V_{DD} granularity and do not rely on off chip DC-DC converters. These proposed architectures instead leverage power switches for dynamic energy reduction.

2.2 Panoptic Dynamic Voltage Scaling

Overview

Panoptic ("all-inclusive") Dynamic Voltage Scaling (PDVS) extends DVFS to finer granularity in and removes the need for DC-DC converter voltage scaling. PDVS, shown in Figure 2–1, modifies the power delivery network by adding multiple PMOS power switches at the component level. This allows each component to select the best V_{DD} from among a discrete set of shared V_{DD} rails (V_{DDH}, V_{DDM}, V_{DDL}) depending on the application requirement. This allows for much more flexible and energy efficient designs [4]. A comparison to recent DVFS processors shows that they are limited by DC-DC converter speed and/or V_{DD} granularity [5][6][7]. PDVS, however, is not limited by DC-DC converter speed or V_{DD} granularity.

Hypothesis

In a full processor, fine grained component dynamic voltage scaling, i.e., PDVS, will lead to near optimal energy efficiency across varying workloads by providing more voltage scaling opportunities due to finer V_{DD} granularity and fast V_{DD} scaling.

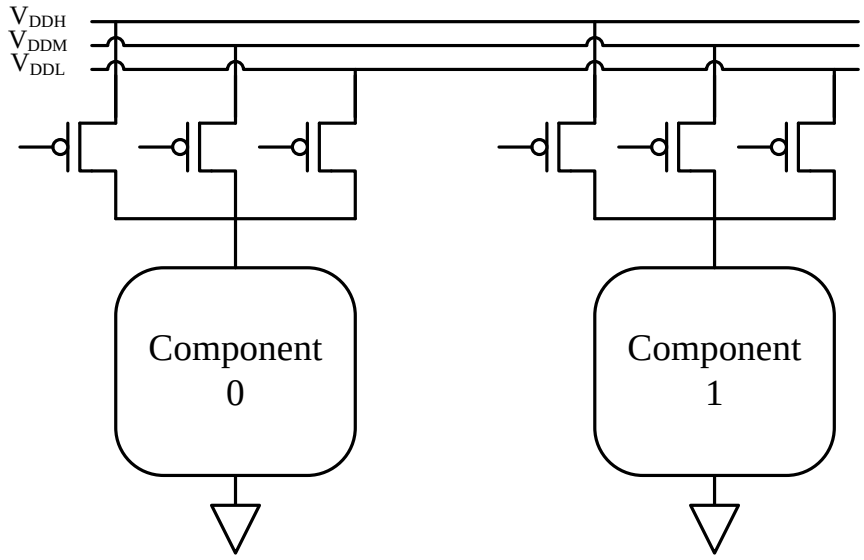

Figure 2–1. Panoptic Dynamic Voltage Scaling

Approach

To demonstrate the benefits of PDVS a 32b data-flow processor was designed and fabricated in a 90nm commercial bulk CMOS process. Figure 2–2 shows a block diagram of this processor as well as the die photo. The PDVS data path consists of: four multipliers and four adders, each with three power switches connected to V_{DDH}, V_{DDM}, V_{DDL}, level converters to prevent shirt circuit energy, a programmable crossbar, a register bank, a 32kb data memory, and a 40kb instruction memory. For fair comparisons, the test chip also included three additional processors, each with a different power delivery network configuration. The first is single-V_{DD}, e.g., all components share a common V_{DD}. The second is multi-V_{DD}, e.g., each component is permanently tied to one of the three available V_{DD}s. Finally, a subthreshold capable PDVS processor was included (discussed further in section 3).

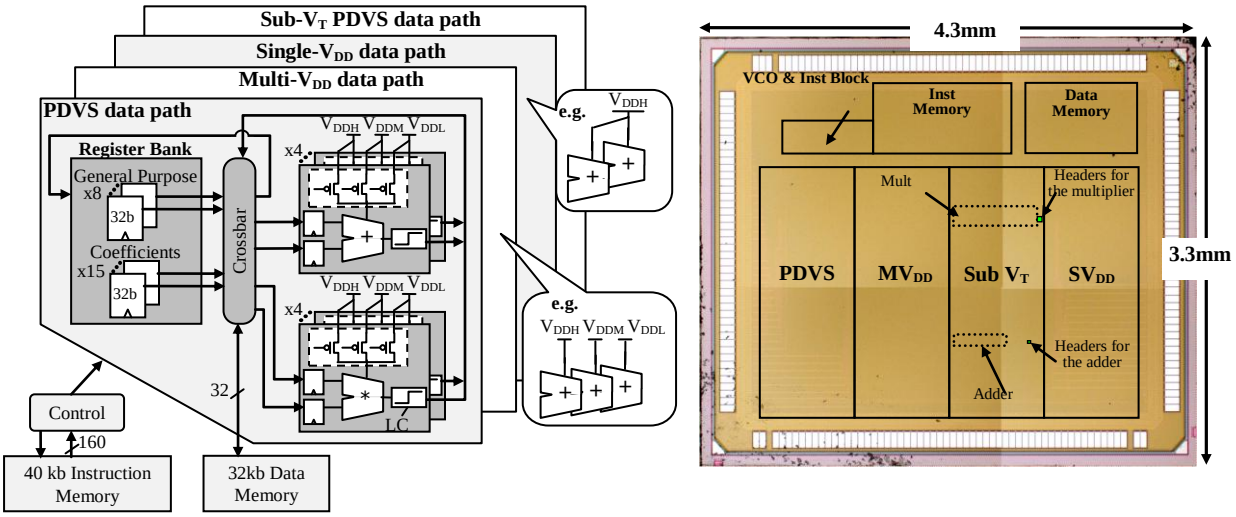

Figure 2–2. (*left*) 32b data flow processors (*right*) chip die photo

2.3 Programmable resistive power grid

Overview

Power gating and dynamic voltage and frequency scaling are two common solutions to reduce leakage energy during standby mode and to improve energy efficiency, respectively. Power gating modifies the power grid by placing large power switches in series with the power supply or ground to collapse the virtual rail and reduce leakage during idle mode. One disadvantage of power gating is that data stored in registers is lost. A variety of approaches to deal with this problem include putting registers on a separate supply, using high V_T balloon registers in parallel with core registers, or other alternative dual V_T register circuits. All of these incur overhead and added design complexity. DVFS during active mode saves power by lowering the frequency and voltage together when timing slack exists. Applying DVFS to multiple blocks requires multiple DC-DC converters that adjust the local voltage levels or alternative schemes that allow local V_{DD} selection from among multiple regulated supplies, such as PDVS. Again, the overhead of these approaches can be substantial. The authors of [6] first introduced separating power gate switches and controlling them individually as a method to reduce noise. This paper expands on this idea and shows how to apply variable weighted power gates in a flexible fashion to provide additional low power operation modes. A variable weighted power gate can provide a controlled power grid resistance to enable a large number of effective voltages at which a component can operate. The block is therefore not constrained by available voltage rails; it can operate at lower voltages than the rest of the system without changing the entire chip V_{DD}, so it avoids the high overhead of extra DC-DC converters. In addition, a

low energy standby mode can be provided that reduces leakage current in idle blocks but enables data retention and incurs lower overhead when returning to normal operation than does full power gating. A similar leakage reduction mode was used to give state retention modes in SRAM arrays [8] for reducing idle power.

Hypothesis

Breaking up a monolithic power gate into independently controlled power gates in parallel allows for a low overhead programmable power grid resistance which provides improved energy efficiency through dynamic energy savings as well as leakage reduction with data retention.

Approach

We propose using a programmable resistive power grid for providing dynamic system level flexibility by partitioning large, monolithic power gating transistors into parallel, independently controllable power gates with different widths, as shown in Figure 2–3. We can leverage this functionality to implement fine grained DVFS at the component level and to enable component level low leakage standby modes with data retention.

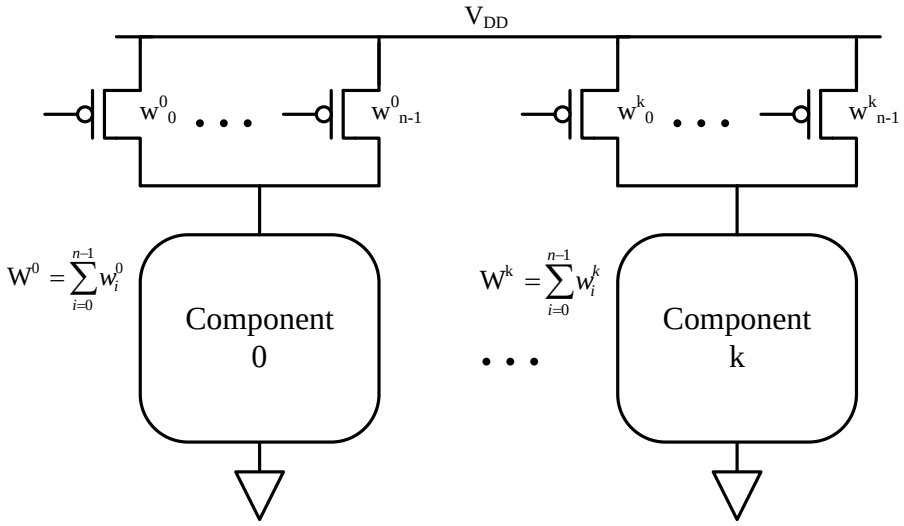

Figure 2–3. Programmable resistive power grid

To highlight the potential energy savings from this scheme, simple modifications can be made to equations eqn. 1–1 and eqn. 1–2

$$\boldsymbol{E_{op\_dynamic}(V_{DD}, V_{rail}) = C_{eff}(V_{rail}) * V_{DD} * V_{rail}} \qquad \textbf{eqn. 2–1}$$

$$\boldsymbol{E_{op\_leakage}(V_{DD}, V_{rail}) = V_{DD} * I_L(V_{rail}) * t_{op}(V_{rail})} \qquad \textbf{eqn. 2–2}$$

As V_{rail} decreases, we expect a greater than linear dynamic energy reduction due to the linear reduction of V_{DD}*V_{rail}, plus a less than linear reduction in C_{eff}, due to device source and drain parasitic junction capacitance being dependent on V_{rail}. Finally, as V_{rail} between V_{rail} decreases, I_L will decrease due to the exponential and the amount of DIBL (drain-induced barrier lowering).

To highlight the potential benefits of leveraging this droop for energy efficiency, we connected a ring oscillator to variable weighted power gates and allowed the rail to settle for each power gate width. Figure

2–4 shows the normalized energy and delay versus the normalized power switch width. As expected, reducing the power switch width decreases the energy and increases the delay. These RO results were confirmed through silicon measurements using a 90 nm commercial bulk technology with four 97 stage ROs in parallel consisting of inverters and delay cells to simulate a high current and activity load. The normalized measured values match the simulated values and show an energy savings of over 30% in silicon.

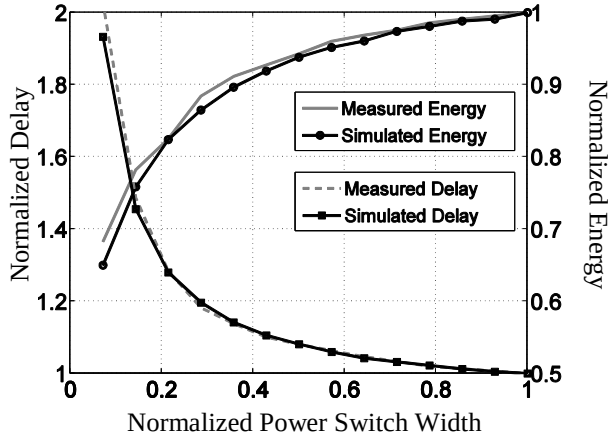

Figure 2–4. Simulated and measured delay and energy for varying power switch width

Many systems and blocks within systems spend large amounts of time idling. Additionally, blocks such as register files or memory may need to retain their data, which is not supported by most power gating schemes. Variable weighted power gates provide a low energy solution that enables data retention with reduced idle leakage current. Leakage current can be reduced through reducing power gate size by dropping the voltage across the active devices which reduces the amount of DIBL, thus reducing device leakage. In Figure 2–5**,** the leakage current is measured for a 32nm SOI four-core x86 processor SOC chip which has a variable weighted power gate ring around the core [8] on silicon hardware. By changing the power gate width by disabling distributed sections of the footer ring via configuration bits, the idle current can be gradually reduced from 100% to a lowest bound of 10%.

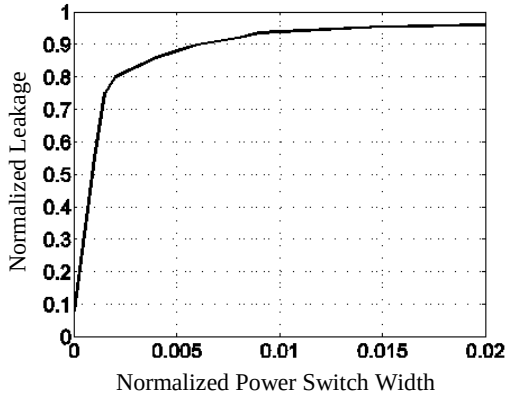

Figure 2–5. Measured leakage with varied power switch width from a 32nm SOI four-core x86 processor

Opportunity for Regulation

In order to assess the benefit of a programmable resistive power grid we investigate the opportunity for dynamic grid voltage control in a commercial x86 four core processor SOC using typical P-state (power

state) occupancy data. A P-state defines a voltage/frequency pair independently for each core in the processor, where P0 is the fastest state and P3 is the slowest. Since all cores share a common V_{DD}, the lowest core P-state sets the operating V_{DD} for all cores, leading to non-optimal V_{DD} for cores with higher P-states. The cores running at a lower P-state V_{DD} than required are only able to use frequency scaling in the absence of a resistive grid. However, Figure 2–6 shows the opportunity for power savings using a programmable resistive power grid. In the figure, the label P1@P0 indicates the total power of core(s) that are running at the P1 frequency while another different core in the SOC is running at a P0 state. During the SysMark trace, the core-wise P-state occupancy is determined by the operating system. By including variable weighted power gates at each core, the cores running at a higher P-state will run at their near optimal V_{DD} during periods of high activity. The figure shows up to ~15% power savings opportunity by using the variable weighted power gate resistive grid technique. Power/performance results can vary depending on the P-state frequency, voltage settings, and the profile of system activity. By allowing individual core-wise voltage settings, the system has more flexibility to differentiate high performance modes from lower performance modes, which can allow opportunity for additional performance boosting when a single core is running at a low P-state.

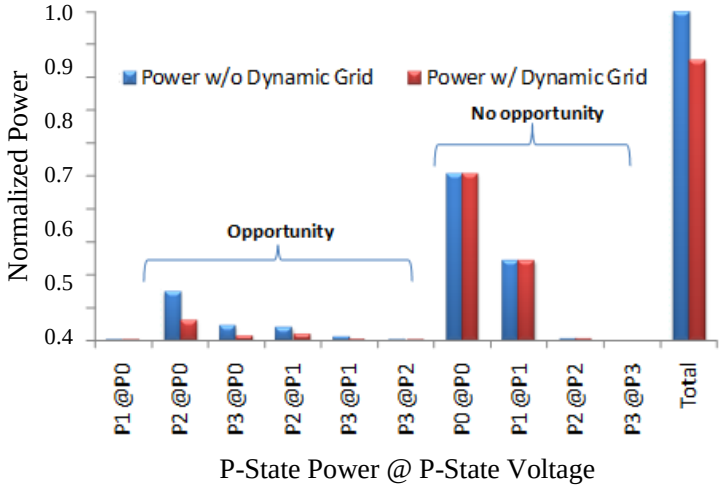

Figure 2–6. Estimated power savings of a four-core x86 processor using a programmable resistive power grid

Core level Modeling

Since the application of this technique requires characterization of the power supply resistance, we propose a design flow, using a commercial power integrity tool, for applying the approach to arbitrary digital designs. We use this design flow to model a full commercial processor using the proposed method for implementing a programmable resistive power grid. A commercial power integrity tool, Apache Redhawk, was used to model the effectiveness of variable weighted power gates as a controlled power supply resistance in a large system. Redhawk was used to model the AMD Bulldozer core [10], which has a similar power gate ring structure seen in [9]. For this simulation, to prevent the simulation time from being prohibitively large, each Route Level Macro (RLM) (roughly 50 in total) in the core was modeled as a time dependent current source and capacitance model, with the exception of the L1 cache and two RLMs without available data. These current profiles were generated from simulations of the Double-precision General Matrix Multiply (DGEMM) benchmark.A simplified package model was included to capture the real RLC effects seen on hardware. Figure 2–7 shows a simplified diagram of the simulation setup.

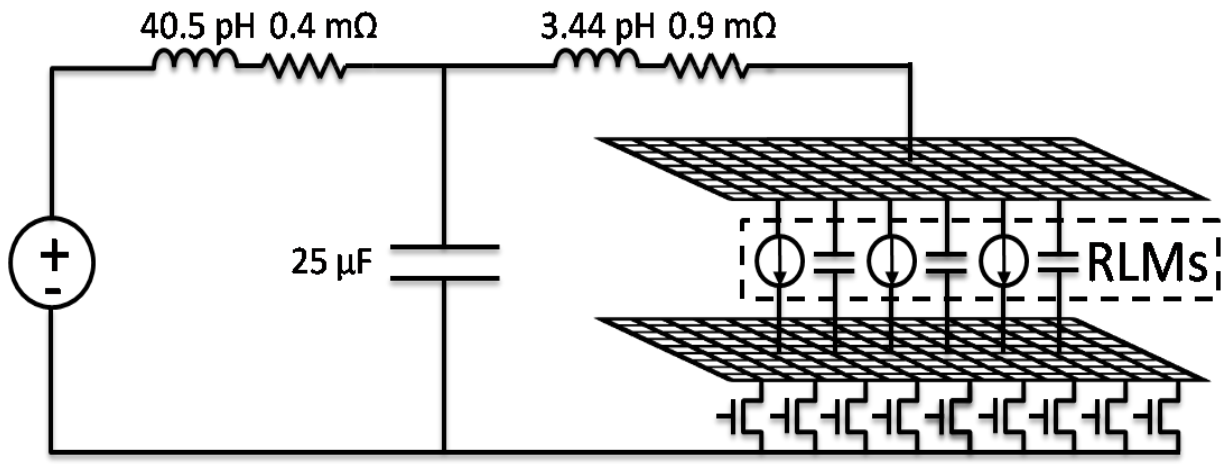

Figure 2–7. Apache Redhawk simulation set for Bulldozer core

Figure 2–8 shows the average V_{DD} response to the applied current models in time, showing that our current model profile was functioning correctly. Figure 12 shows the V_{DD} and virtual-V_{SS} voltage profile over time for different normalized power gate widths. Notice that at 5.07%, the virtual-V_{SS} is only slightly above the 100% case, which is expected for a power gate ring system designed for a high performance core. This figure also includes every RLM's V_{DD} and virtual-V_{SS} superimposed into a single graph. The negligible variance in V_{DD} and virtual-V_{SS} between RLMs across the chip is due to the robust power grid with low resistance showing that the dominant factor in the virtual-V_{SS} droop is caused by the controlled power supply resistance of the power gates. Through variable weighted power gates, we are able to achieve a wide range of virtual-V_{SS} supplied to the core.

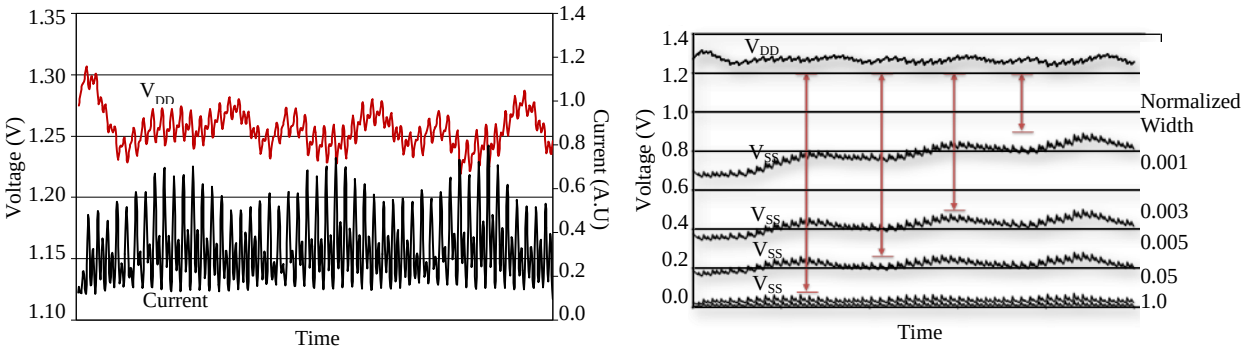

Figure 2–8 (left) V_{DD} and current respone from Redhawk (right) V_{DD} and virtual-V_{SS} profile over time

2.4 Proposed contributions

- First processor implementing PDVS
- Methodology for header sizing for nominal V_{DD}s
- Programmable power delivery network allowing for better V_{DD} granularity for multicore systems
- Model for implementing and demonstrating a programmable resistive power grid

3. Enabling subthreshold mode

A previously mentioned a major focus of in academia has been subthreshold digital operation. That is to use a V_{DD} for the entire circuit that is below the threshold voltage of the device. The threshold voltage (V_T) is defined as the transistor gate to source voltage differential (V_{GS}) that allows the transistor to begin conducting current. When V_{GS} is below V_T, the transistor is off, though there is still enough current to perform digital operations. Enabling subthreshold operation in conventional architectures is non-trivial. For the context of this work we will focus on architectural organizations as well as power delivery network optimizations to enable subthreshold in the context of PDVS. These same concepts are generally applicable to all architectures however.

3.1 Architecture optimizations

Overview

Panoptic ("all-inclusive") Dynamic Voltage Scaling (PDVS) extends DVFS to finer granularity in and removes the need for DC-DC converter voltage scaling. PDVS, shown in Figure 2–1, modifies the power delivery network by adding multiple PMOS power switches at the component level. This allows each component to select the best V_{DD} from among a discrete set of shared V_{DD} rails (V_{DDH}, V_{DDM}, V_{DDL}) depending on the application requirement. PDVS was initially constrained to have V_{DDH}, V_{DDM} and V_{DDL} all be super threshold voltages. Simply lowering V_{DDL} to V_{SUBVT} would not work. First, as was shown in Figure 2–2, the PDVS architecture has level converters that only work with super threshold V_{DD}s. Second, PDVS provides fast V_{DD} scaling at the component level between V_{DD}s, but as discussed subthreshold hold operation is exponentially related to V_{DD} and is much slower than super threshold operation. This implies that subthreshold operation should be considered a mode change that stays in the subthreshold mode for extended periods of time. Finally, for the best energy efficiency, all processor components need to be in subthreshold, not just adder and multipliers.

Hypothesis

Architecture techniques can be implemented to provide PDVS a subthreshold mode of operation to improve energy efficiency when application allow.

Approach

We propose specific design changes to the data path to optimize for subthreshold operation. First, we propose to use a subthreshold optimized level converter [11] to communicate to the memories and IO which are still operating at super threshold V_{DD}s. As previously mentioned, the level converters already in the data path are not capable of operating in subthreshold. Therefore, we propose using a bypass and power gate scheme when the level converters are not needed. The level convert and bypass scheme are shown in Figure 3–1(a). A similar scheme is used with the subthreshold level converters communicating to the memories and IO, when not used, they are power gated and bypassed. Second, power switches are added to the other architecture components (register file, crossbar) to allow the entire data path to operate in subthreshold when performance requirements allow for a subthreshold mode change (Figure 3–1(b)).

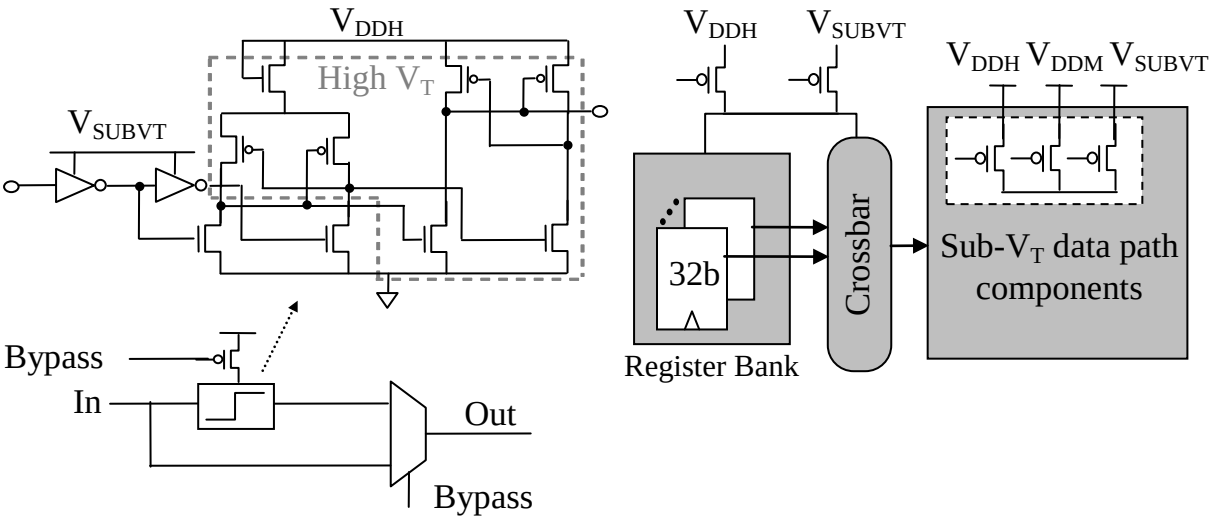

Figure 3–1. PDVS subthreshold optimizations. (a) Subthreshold level converter [11] and level converter bypass. (b) Power switches on register file and cross bar to lower into subthreshold

3.2 NMOS as Subthreshold header

Overview

As proposed PDVS uses multiple voltage supplies at high, middle and low values (V_{DDH},V_{DDM}, V_{DDL}) with PMOS power switches to select the appropriate V_{DD} for different fine grained blocks/components in the design depending on local application requirements. PDVS supports DVFS, power gating for leakage reduction, and subthreshold operation when appropriate. The introduction of a power switch device in the power delivery network creates an IR drop across the header resulting in a reduced virtual-V_{DD} value and performance degradation. Power switch sizing is critical to maintain energy efficiency. An undersized power switch results in large performance degradation, however an oversized power switch results in increased leakage and increased area overhead. For a subthreshold voltage rail, we propose using a NMOS transistor as a header instead of a PMOS. Power switch sizing methodologies have been examined in depth to support techniques like multi-threshold CMOS (MTCMOS) and power gating [13]-[17]. To compare our proposed power switch against the conventional we use a common power switch sizing methodology that sets the power switch size such that the critical path meets an acceptable delay degradation from the nominal case (i.e., no power switch). The allowable degradation is a design choice chosen by the system designer.

Hypothesis

For designs using PMOS power switches to select between multiple voltage rails, such as PDVS, or for power gating, we propose using an NMOS based header with a nominal V_{DD} gate control. For designs with flexible V_{DD}s, a transmission gate power switch provides the most robust header configuration.

NMOS as a Subthreshold Header

Figure 3–2 shows the conventional subthreshold power switch architecture as well as the proposed NMOS power switch architecture. The conventional architecture uses a PMOS power switch with the body tied to virtual-V_{DD} to avoid reverse body bias [12]. Since the PDVS architecture has multiple supplies, the power switch control signals are full swing, up to V_{DDH}. For the conventional PMOS power switch this provides a strong turn off of the off headers. In the proposed alternative, an NMOS device with its body tied to ground is used as the header between the subthreshold rail and the component.

During subthreshold operation (i.e., only V_{SUBVT} enabled) the conventional PMOS power switch has a $|V_{GS}| = V_{SUBVT}$, however the proposed NMOS power switch has a $|V_{GS}|=V_{DDH}-V_{SUBVT}$. The higher $|V_{GS}|$ of the NMOS device provides a much higher current than the PMOS, since the NMOS is in the linear region of operation while the PMOS is in the cutoff/subthreshold region of operation. The higher current from the NMOS device provides a more stable virtual-V_{DD} for a much smaller transistor.

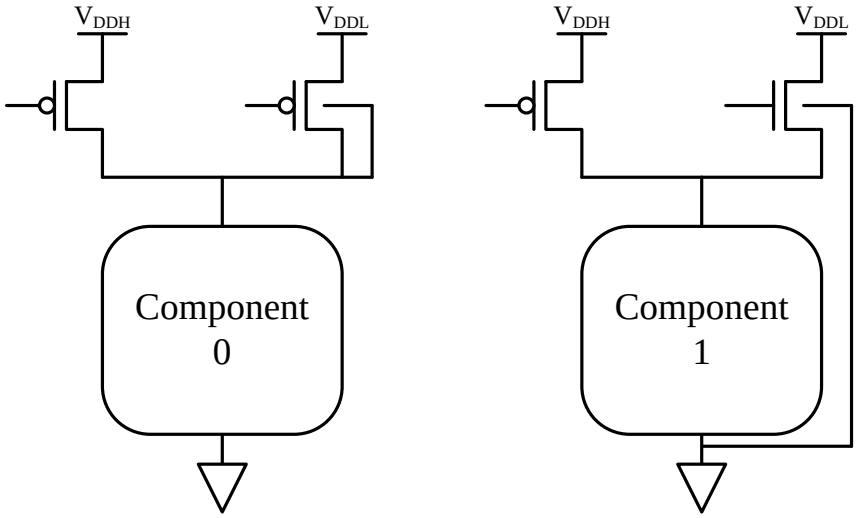

Figure 3–2. (*left*) conventional PMOS power switch (*right*) proposed NMOS power switch

Simulation results

We used a commercial 130nm bulk process to simulate, measure, and compare the conventional and proposed subthreshold header topologies. To provide a flexible, representative load circuit we used ten 27-stage ring oscillators (ROs) in parallel, with each RO capable of being enabled independently. To simplify the comparison, each block of parallel ROs only had two header power switches as shown in Figure 3–2. In simulation, we swept the widths of the headers to examine the impact of size on header behavior, while in the test chip we included programmable sized headers for flexible measurements. Figure 3–3 demonstrates the impact of power switch width on virtual-V_{DD} for two different activity factors. An activity factor of 1.0 corresponds to all 10 ring oscillators enabled in parallel while 0.1 corresponds to only 1 ring oscillator enabled. These two activity factors represent the upper and lower bounds in this design. V_{SUBVT} was set to 0.3V, well below the threshold voltage in the technology. Across the wide range of sizes used, the NMOS is able to maintain virtual-V_{DD} at the target 0.3V due to the NMOS being in the linear operating region. The PMOS, however, is unable to maintain virtual-V_{DD} at the target 0.3V for small widths since it is in the subthreshold operating region. It is necessary to keep the virtual-V_{DD} near the target V_{DD} since frequency depends exponentially on the virtual-V_{DD} voltage in subthreshold, so any IR drop in the power delivery network leads to huge performance decreases (). The impact of the power switch width on oscillator frequency is shown in Figure 3–3.The frequency has been normalized to the frequency at 0.3V without power switches. With near minimum sizing at the lowest activity factor the NMOS has a worst case frequency degradation of only *3%*, while the minimum PMOS has a worst case frequency degradation of *88%*. At the highest activity factor with near minimum sizing the NMOS has a worst case frequency degradation of *16%*, while the smallest PMOS has a worst case frequency degradation of *93%*. Using the traditional sizing methodology and a target delay degradation of

10%, the required NMOS size is approximately *280X smaller* than a PMOS for the same target degradation at the same worst case activity factor, with sizes of 640nm and 180µm respectively.

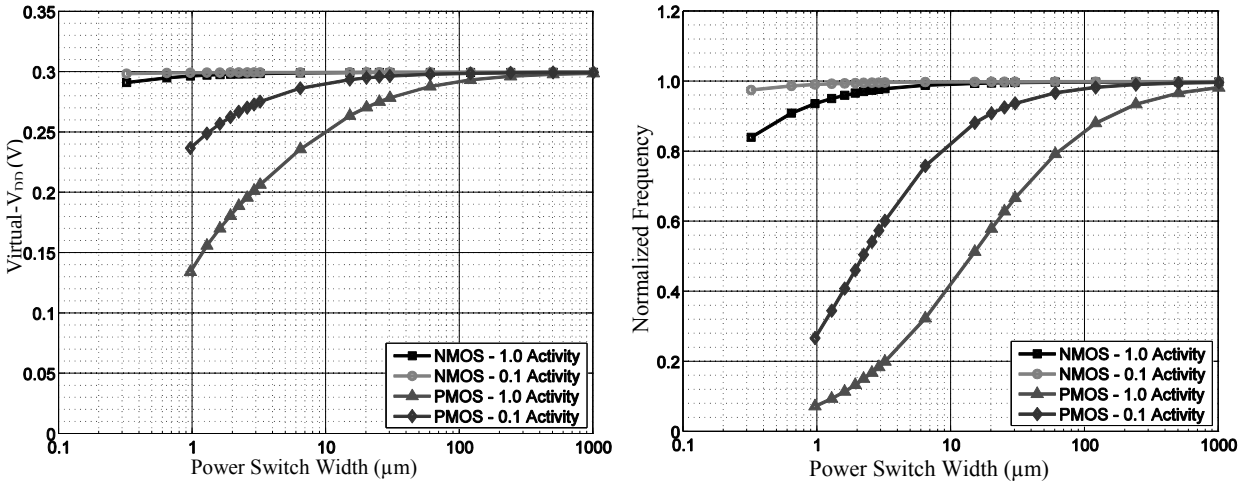

Figure 3–3. (*left*) Virtul-V_{DD} vs power switch width for proposed and conventional power switches (*right*) Frequency vs power switch width for proposed and conventional power switches

The total energy per operation while operating at V_{SUBVT} is defined by the following equation:

$$E_{op} = E_{DYN_{VSUBVT}} + E_{LEAK_{VSUBVT}} + E_{LEAK_{VDDH}} \qquad \textbf{eqn. 3–1}$$

This includes the overheads of the PDVS architecture associated with having multiple V_{DD}s and power switch devices. Simulated energy per operation versus power switch width for an activity of 1.0 is shown in Figure 3–4. For both NMOS and PMOS, the energy is normalized to the same value; the energy per operation with no power switches. The shift in energy above the nominal for each of these designs is due to overheads inherent in the PDVS architecture. Specifically, the increase in energy comes from E_{LEAK} through the off V_{DDH} power switch while the V_{SUBVT} power switch is on. The decrease in energy as power switch size is reduced is due to the IR drop across the power switch, which lowers the dynamic energy. However for the PMOS design, the energy starts to increase at the lower widths due leakage becoming the dominate factor because of lower operating frequencies.

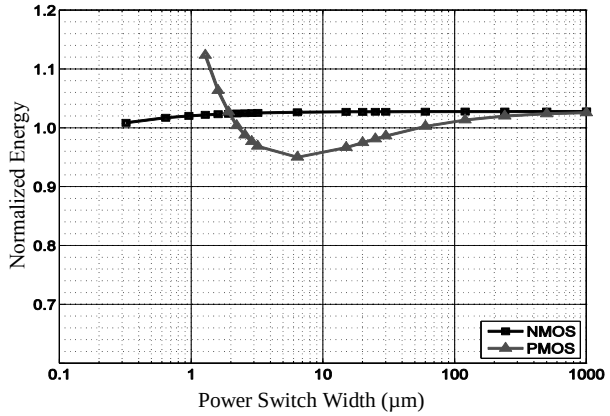

Figure 3–4. Normalized Energy per op vs. power switch width

At these lower widths, the virtual-V_{DD} becomes much lower, resulting in initially lower dynamic and total energy as discussed, As the width is reduced further the frequency becomes so slow which results in E_{LEAK} through the V_{DDH} and V_{SUBVT} power switches becoming dominate causing an increase in total energy. The use of an NMOS power switch does not adversely increase the overheads associated with the PDVS architecture or have a higher energy per operation than a PMOS power switch. Gate leakage for this technology was not a concern; at the largest power switch size of 1mm, the gate leakage energy was only 0.04% of the total energy.

Transmission gate for flexible design

If the V_{SUBVT} rail is kept at a subthreshold voltage and NMOS power switch should be used. However, if the rail needs to be a flexible and encompass a wide range of V_{DD}s, the NMOS fails as a power switch at V_{DD}s above V_T due to the V_T drop seen across the NMOS. For such designs that require a wide range of voltages on the V_{SUBVT} rail, we propose to use a transmission gate architecture shown in Figure 8. When V_{SUBVT} is near- or subthreshold, the NMOS will be the dominate device. Conversely, when in voltages above V_T, the PMOS will be the dominate device. As shown by the ring oscillator energy-delay curves in Figure 3–5, this leads to the most optimal header configuration. At higher VDDs the NMOS is not capable energy efficient high performance. The transmission gate (dominated by the PMOS) is 21% lower energy than the NMOS for the highest performance (lowest delay) capable of the NMOS. However the PMOS is not capable of energy efficient lower performance. The transmission gate (dominated by the NMOS) is 33% faster for the same energy.

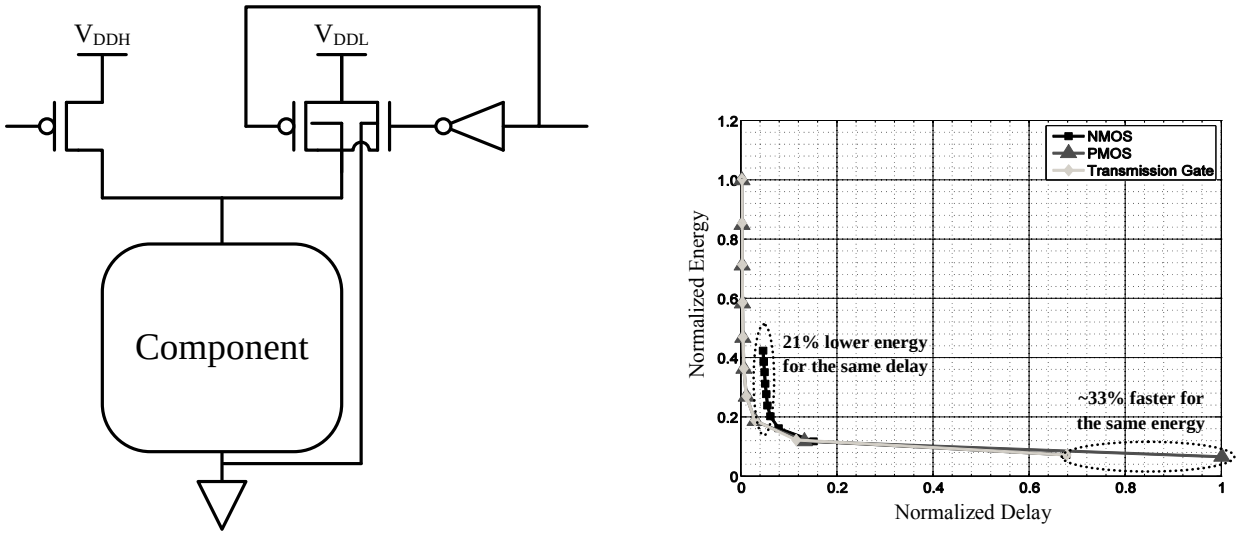

Figure 3–5. (*left*) Proposed transmission gate architecture (*right*) Energy delay curve of NMOS, PMOS and transmission gate based power switch

3.3 Proposed contributions

- Methodology for adapting PDVS for sub-threshold operation
- Proposed use of NMOS as subthreshold header. Proposed use of transmission gate for flexible designs.
- Analytical comparison between the use of PMOS and NMOS headers across V_{DD} for varying current loads.

4. Power delivery network analysis

Two related key design challenges in the power delivery network are di/dt noise and uncontrolled IR drop. Di/dt noise can occur with high frequency operation as well as when a power gated component is reconnected to V_{DD} (i.e., power gate turned back on). With respect to power gating there is a large rush current that is associated with returning the collapsed virtual-V_{DD} to the nominal voltage. Since the power delivery network consists of many intrinsic resistances, inductances and capacitances this rush current creates a di/dt noise that will impact voltage margins and lead to less optimal designs. As previously discussed, one cause of IR drop is undersized power switches. Another cause of IR drop can be an insufficiently designed power grid.

4.1 Panoptic Dynamic Voltage Scaling

Overview

The physical implementation of PDVS can lead to increased di/dt noise and IR drop than a comparable design with a single V_{DD}. For a comparable design, roughly the same amount of metal that was used for signal routing and V_{DD}/V_{SS} power grid now has to be used for signal routing and V_{DDH}, V_{DDM}, V_{DDL}, V_{SS} and virtual-V_{DD} power grids. This will increase the power grid resistances, as well as decrease the power grid capacitance. Like power gating, PDVS has rush current associated with returning a collapsed virtual-V_{DD} to V_{DDH} if the component was power gated, but also has rush current associated with changing from a lower V_{DD} to a higher one.

Hypothesis

Power grid design for PDVS will not need to be uniform across V_{DDH}, V_{DDM} and V_{DDL} and with minimal overheads di/dt noise and IR drop can be mitigated. Specifically, the design requirements for power grids for lower voltages will not be the same as for high voltages due to the lower load current.

Approach

In order to fully explore the physical implementation impact of the PDVS architecture, we plan to use synthesis and place and route tools instead of custom layout. This allows us to create and test designs much faster. The synthesis and place and route flow is shown in Figure 4–1. Synthesis is the process of translating behavior register transfer logic (RTL) to structural RTL. Place and route is the process of translating the structural RTL into physical layout. The tools used for synthesis and place and route are Cadence RTL Compiler (RC) and Cadence Encounter, respectfully.

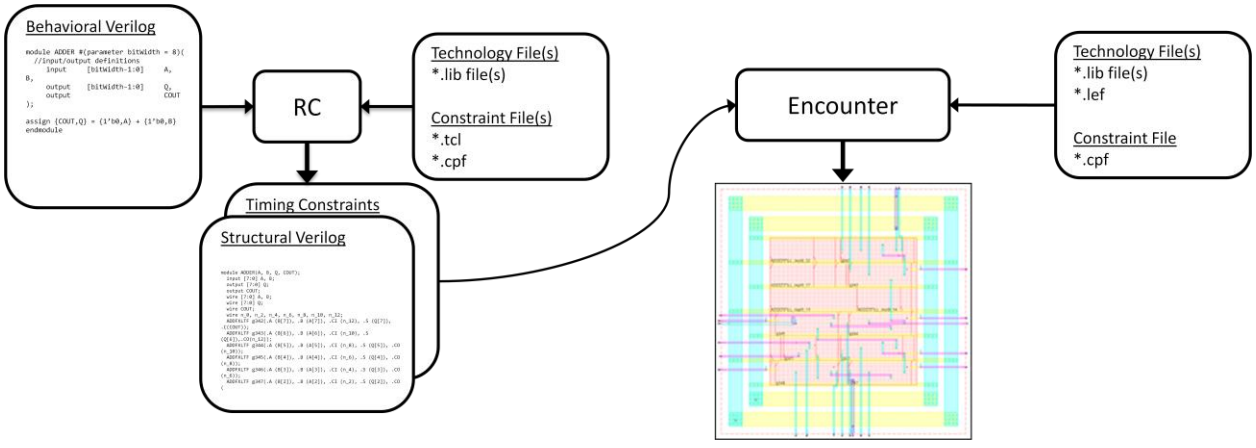

Figure 4–1. Synthesis and place and route flow

The biggest drawback of using this flow is the tools limited energy efficiency capabilities. RTL inherently does not have any power information. The tools provide the ability to add power information for RTL through the use of a common power format (cpf) constraint file. This allows us to set different V_{DD} domains, as well as power gate and clock gate our design to improve energy efficiency. PDVS however is not natively supported. Therefore, the first step for this analysis will be to modify the synthesis and encounter flow to allow for a PDVS implementation.

Modify synthesis and place and route

As mentioned the native RC and Encounter do not support a PDVS implementation. However, with the use of the CPF file it does support power gating. Through careful manipulation of the CPF file and encounter placement scripts, I should be able to get a functioning PDVS implementation to work. Preliminary work has been completed to suggest a PDVS workaround is possible, but not yet fully functional. As a proof of concept we took an 8 bit PIC processor, and implemented PDVS on the ALU unit. Figure 4–2(a) shows this block diagram, while Figure 4–2(b) shows the physical implementation. Annotated in (b) are the power switches for V_{DDH}, V_{DDM} and V_{DDL} for the ALU of the PIC.

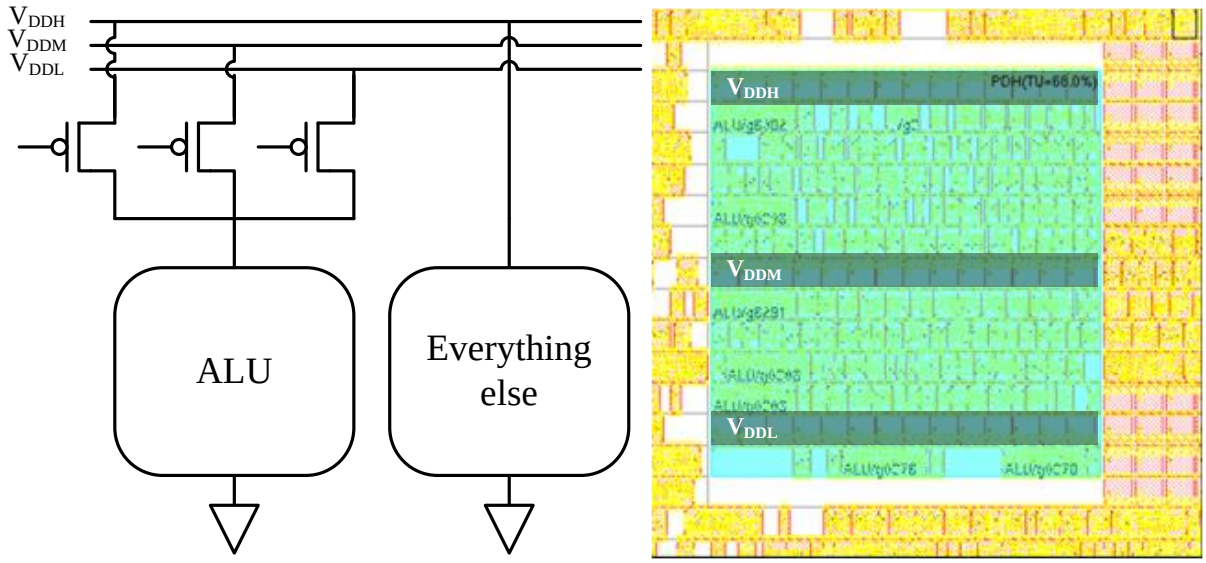

Figure 4–2. RC and Encounter PDVS proof of concept (a) architecture overview (b) physical implementation with annotated power switches

Comparison

Power delivery network analysis will be done through a tool called Encounter Power System (EPS). This tool allows for static and dynamic IR analysis as well as rush current analysis. With EPS we will be able to characterize the impacts of PDVS on the power delivery network. To demonstrate the usefulness of EPS, we took the PIC processor and placed and routed it with a power gate. Figure 4–3 shows the IR drop output from EPS. With EPS we are able to see the locality of the IR drop, as well as the magnitude. To assess the impact of PDVS, we will perform a sensitivity analysis of IR drop and noise with respect to V_{DD}, power grid metal area, and decoupling capacitance. This analysis will be compared to the same design without PDVS as well as a design that is only power gated, in order to analysis the added IR drop and noise introduced with PDVS.

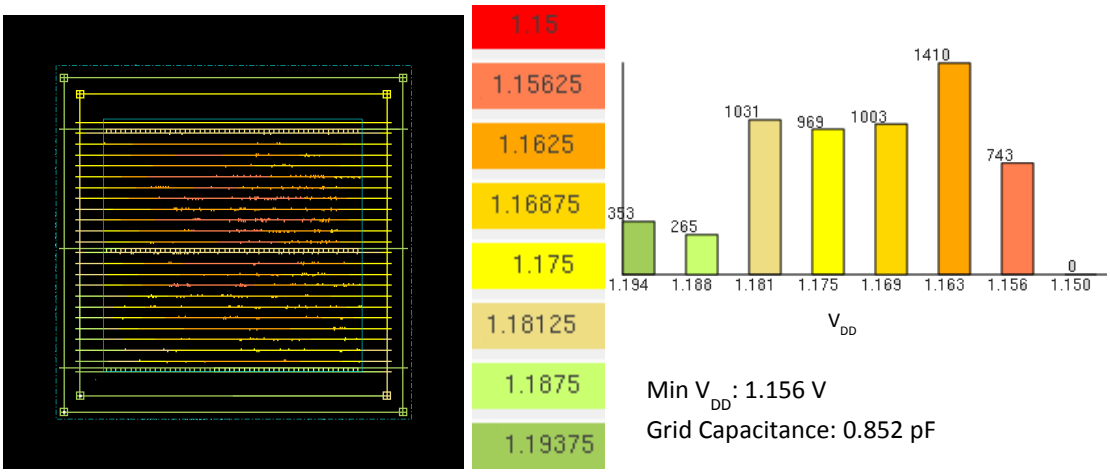

Figure 4–3. IR map and V_{DD} histogram of a power gated PIC core from EPS

4.2 Field programmable core array (FPCA) impact on power delivery network

Overview

Field Programmable Core Array (FPCA) supports a reconfigurable system capable of variable-width SIMD and change between SIMD and MIMD configurations according to application demands. This is achieved by reducing a scalar processor core into a front end (FE) and a processing element (PE). For example, in order to achieve variable-width SIMD, a varying number of PEs can be connected to a single FE. Through various combinations of FE and PE connections, a network on-chip (NoC) is made. A simplified block diagram of this system is shown in Figure 4–4.

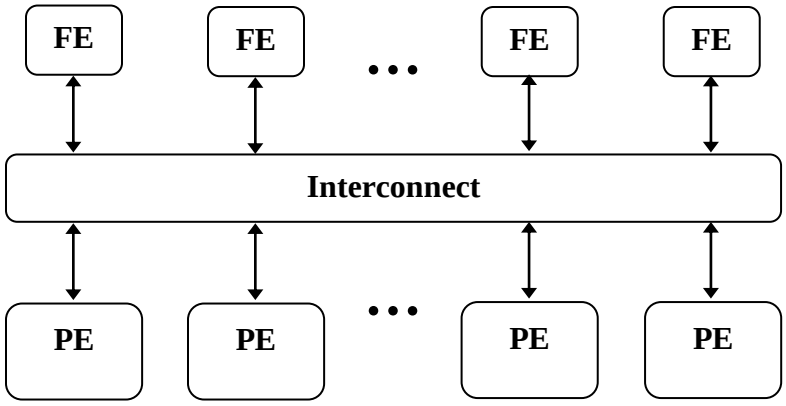

Figure 4–4. Proposes FPCA overview

Hypothesis

Dynamic reconfigurable architectures, such as FPCA, can create prohibitive power delivery network noise that will limit the performance of these designs. A methodology for analyzing this impact is needed in order to fully understand the benefits of these architectures.

Approach

A similar methodology will be used for this analysis that will be used for the PDVS power delivery network noise analysis. Cadence RC will be used for synthesis of a variable width SIMD architecture, Cadence Encounter will be used for place and route, and finally Cadence EPS will be used to analysis the power delivery network. The power delivery network will be compared to a similar design without variable width SIMD.

Tiled hierarchical implementation

Implementation of FPCA is straight forward compared to PDVS. However a new hierarchical design flow has to be incorporated for such a large design. For a design with 8PE's and 8FE's the design time would be prohibitively large and not scalable to any larger configurations. To get around this we create FE/PE tiles called interface logic modules (ILMS), shown in Figure 4–5. With the ILMs the FE/PE only needs to be designed once, reducing the total design time. Figure 4–6 shows two floorplan views using the FE and PE ILMs. With this flow we will be able to perform a power delivery network noise sensitive analysis for the number of FEs and PEs.

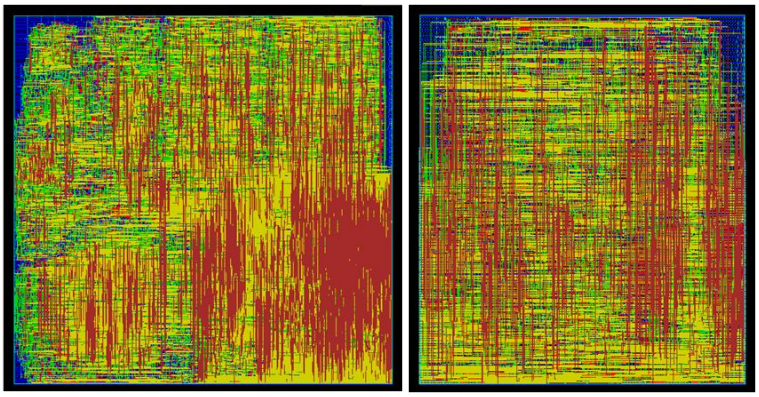

Figure 4–5. (*left*) PE ILM, (*right*) FE ILM (not to scale)

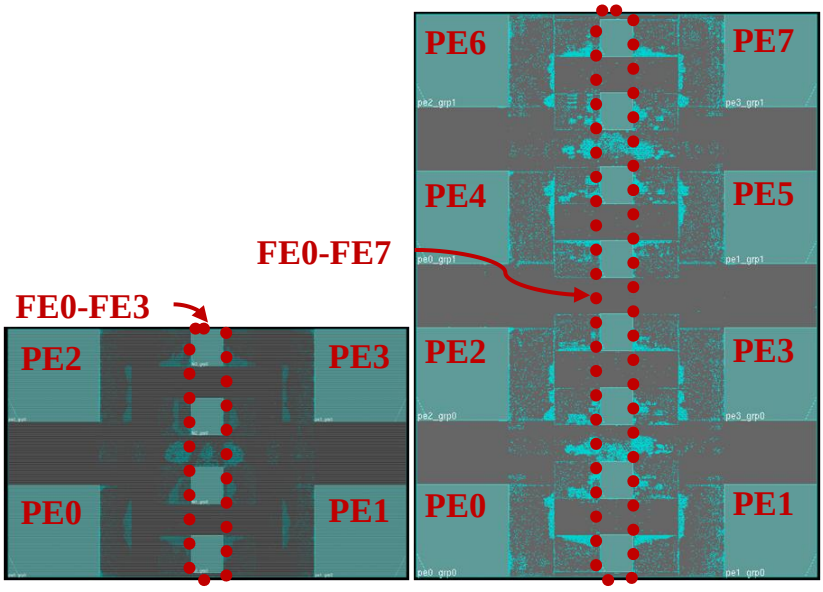

Figure 4–6. Floorplan view of (*left*) 4FE4PE and (*right*) 8FE8PE

4.3 Proposed contributions

- Analysis and methodology for characterizing power delivery network properties associated with implementing PDVS, specifically:
  - IR drop due to reduced metal area in power delivery network
  - di/dt due to rush current switching headers
- Power grid design methodology for varied voltages
- Methodology for characterizing the power delivery network for reconfigurable architectures

5. Research Platform

5.1 Scripted infrastructure

Overview

One of the major challenges faced in our research group is a lack of infrastructure support when implementing energy efficient designs. As previously mentioned, the current synthesis and place and route tool flow only allows for basic energy efficient design. The tools support multi-V_{DD} domains, power gating and clock gating. For academic research, a more robust tool flow is needed to explore the design trade-offs of energy efficient power delivery networks.

Hypothesis

A robust scripted tool flow will allow for better design space exploration with regards to energy efficient power delivery network design.

Approach

As mentioned, the current tool flow has limited energy efficient design options. Specifically the tool flow allows for power gating, clock gating and multi-V_{DD}. The flow does not inherently support any of the proposed energy efficient designs (PDVS, NMOS power gate & Resistive power grid). In order to implement these energy efficient designs, we propose to make modifications to the existing tool.

One of the main goals of this infrastructure is to be an easy to use tool that aids in our groups research. For this reason, the tool that we will develop will be user friendly as well as extendable to allow for the inclusion of future energy efficient design implementations.

The infrastructure will be based on the TCL language for running the Cadence design tools as well as perl as a system driver to provide the most flexibility.

5.2 Proposed contributions

- An energy efficient design tool allowing for quick and easy low power design at UVa and general public. The current EDA tools are general very cumbersome, this tool will be easier to use as well as provide non tradition lower power techniques. Will focus on using the Cadence for implementing standard low power techniques such as:
    - Power gating
    - Clock gating
    - Multi-V_{DD}

  As well as adapting the Cadence tools to allow for proposed techniques such as:
    - PDVS
    - NMOS power gate
    - Resistive Power Grid

6. Research tasks

Subject	#	Task description	Status	Related publications
PDVS	1	Design space exploration	Completed	
	2	Simulation	Completed	
	3	Layout	Completed	
	4	Chip testing	Completed	KAC1, KAC2, KAC3
	5	Subthreshold testing	Sep-2012	KAC7
	6	Synthesis, place and route, noise analysis	Apr-2013	KAC9, KAC10
Resistive power grid	7	Design space exploration	Completed	
	8	Redhawk Modeling	Completed	KAC4
	9	Layout - from AMD internship	Completed	
	10	Layout - from BSN2	Nov-2012	
	11	Testing AMD chip	? Still waiting on silicon	
	12	Testing BSNrev2	Jun-2013	KAC8, KAC10
NMOS Header	13	Design space exploration	Completed	
	14	Simulation	Completed	
	15	Layout	Completed	
	16	Chip testing	Completed	KAC5, KAC10
Field Programmable Core Array	17	Design space exploration	Completed	
	18	Synthesis, place and route, noise anlysis	May-2013	KAC11, KAC12
Energy efficient design tool	19	Add support for conventional (clock gating, power gating, multi-VDD)	Nov-2012	
	20	Add support for proposed (PDVS, resistive power grid, NMOS header)	Nov-2012	
	21	Add support for Encounter Power System	Jan-2013	KAC13

7. List of publications

[KAC1] Shakhsheer, Y., S. Khanna, **K. Craig**, S. Arrabi, J. Lach, and B. H. Calhoun, "A 90nm Data Flow Processor Demonstrating Fine Grained DVS for Energy Efficient Operation from 0.25V to 1.2V", *Custom Integrated Circuits Conference*, San Jose, 09/2011.

[KAC2] Calhoun, B. H., S. Arrabi, S. Khanna, Y. Shakhsheer, **K. Craig**, J. Ryan, and J. Lach, "REESES: Rapid Efficient Energy Scalable ElectronicS", *GOMAC Tech*, 03/2010.

[KAC3] Khanna, S., **K. Craig**, Y. Shakhsheer, S. Arrabi, J. Lach, and B. Calhoun, "Stepped Supply Voltage Switching for Energy Constrained Systems", *ISQED*, 2011.

[KAC4] **Craig, K**., Y. Shakhsheer, S. Khanna, S. Arrabi, J. Lach, B. H. Calhoun, and S. Kosonocky, "A Programmable Resistive Power Grid for Post-Fabrication Flexibility and Energy Tradeoffs", *International Symposium on Low Power Electronics and Design*, 2012.

[KAC5] **Craig, K**., Y. Shakhsheer, and B. H. Calhoun, "Optimal Power Switch Design for Dynamic Voltage Scaling from High Performance to Subthreshold Operation", *International Symposium on Low Power Electronics and Design*, 2012.

[KAC6] Calhoun, B. H., Y. Zhang, S. Khanna, **K. Craig**, Y. Shakhsheer, J. Lach, "A Sub-Threshold FPGA: Energy-Efficient Reconfigurable Logic."*GOMACTech*. March 2011.

Anticipated publications

[KAC7] PDVS JSSC journal paper

[KAC8] BSN revision2 paper.

[KAC9] PDVS noise analysis

[KAC10] Subthreshold power grid design methodologies

[KAC11] Variable width SIMD paper

[KAC12] Reconfigurable architecture noise analysis

[KAC13] Energy efficient tool paper

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